REMARKS

Reconsideration and reexamination of this application in light of the above-amendments and the following remarks is respectfully requested. Claims 1-4, 7-8, 11-16, 19-20, 22-25, and 27-28 are pending in this application. By way of this response Claims 1, 3, 11-13, 15, 20, 22, 24, and 28 have been amended. Support for the amendment can be found throughout the specification and drawings as filed. No new matter has been added. Reconsideration of the rejections set forth in the outstanding Office Action is respectfully requested in view of the following remarks.

I. Telephonic Interview

Applicant thanks the Examiner for the courtesies extended during the telephonic conference conducted on July 1, 2003. While no agreement was reached, Applicants have considered the Examiner's comments in responding to the Office Action. Accordingly, reconsideration of the rejections set forth in the present Office Action is respectfully requested in view of the preceding amended claims and the following remarks.

II. Information Disclosure Statement

An IDS has been filed with this amendment. The IDS includes a US patent granted to Degani et al (US5646828) that applicant believes corresponds to the Degani et al (Japanese Application #08-036034) reference cited by the Examiner.

III. Rejection Under 35 U.S.C. §102(b), Degani reference

Claims 1-4, 7-8, 11-16, 19-20, 22-25, and 27-28 stand rejected under 35 U.S.C. §102(b) as being anticipated by Degani et al (Japanese Patent Application #08-036034) and as shown in figure 7A of Kimura (US Patent Application #2002/0175421A1. Applicant traverses this §102(b) rejection in light of the claims as amended.

Claims 1-4, 7-8, 11, 22-25, 27, and 28 are directed to aspects of an integrated chip package and Claims 13-16 and 19-20 are directed to a method of forming an integrated chip package.

The subject matter encompassed by Applicant's Claims 1-4, 7-8, 11, 13-16, 19-20, 22-25, 27, and 28 includes an integrated chip (IC) package in which an intermediate substrate is arranged above a planar package substrate and electrically connected to the planar package substrate. This is supported throughout the specification and figures including figure 1. The IC package also includes a heat sink having side portions that extend

towards the planar package substrate. This is also supported throughout the specification and figures.

In contradistinction, Degani shows an integrated chip package having a package substrate with a cavity within which an intermediate substrate or semiconductor chip is arranged (see figures 1-10). Degani does not show a planar package substrate, instead Degani shows a package substrate having a cavity within which other assemblies such as the intermediate substrate or a semiconductor chip are arranged.

Figures 1-6 and 9-10 of Degani show the intermediate substrate located within a package substrate cavity. Degani does not show arranging the intermediate substrate above the package substrate. In addition, in Figures 7 and 8 of Degani where a semiconductor chip is arranged within the package substrate cavity and the intermediate substrate is arranged below the package substrate, the cover 75 (which may also be a heat sink) is mechanically coupled to the intermediate substrate. The heat sink does not connect to the semiconductor chips which are located on the other surface of the intermediate substrate. Whereas the subject matter encompassed by Applicant's Claims 1-4, 7-8, 11, 13-16, 19-20, 22-25, 27, and 28 includes a heat sink that is thermally coupled to the semiconductor chips.

The arguments presented for Degani also apply to Kimura, since Figure 7A of Kimura shows Figure 1 of Degani.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of these rejections under 35 U.S.C. §102(b) of independent claims 1, 13, and 22 as well as dependent claims 2-4, 7-8, 11, 14-16, 19-20, 23-25, 27, and 28.

IV. Rejection Under 35 U.S.C. §102(b), Kurokawa reference

Claims 1-4, 7-8, 11-16, 19-20, 22-25, and 27-28 also stand rejected under 35 U.S.C. §102(b) as being anticipated by Kurokawa (US Patent #5291064). Applicant traverses this §102(b) rejection in light of the claims as amended.

Kurokawa shows a packaged semiconductor device including an intermediate substrate connected to an alumina package 47 (see figure 6). The package 47 is not planar, instead the package 47 has side portions projecting towards a heat sink 45. In addition, the intermediate substrate is not above the package 47, but instead within the package 47 between the side portions. Also, the heat sink 45 is shown as a planar structure extending between the side portions of the package 47. The heat sink 45 does not include side portions extending towards the package 47.

In contradistinction, Applicant's claimed subject matter of Claims 1-4, 7-8, 11, 22-25, 27, and 28 includes a planar package

substrate connected to the intermediate substrate and a heat sink having side portions extending towards the planar package substrate.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of this rejection under 35 U.S.C. §102(b) of independent claims 1, 13, and 22 as well as dependent claims 2-4, 7-8, 11, 14-16, 19-20, 23-25, 27, and 28.

V. Conclusion

Applicant has carefully reviewed each of the objections and rejections set forth by the Examiner and has amended the claims as indicated herein to individually address the Examiner's rejections and objections and to place all claims in condition for allowance. Applicant submits that the specification and drawings are in order and that all of the claims are now in condition for allowance. Such action is respectfully requested. A check in the amount of $110 is enclosed in payment for a one month extension of time. Please apply any other charges or credits to Deposit Account No. 50-1236. If the Examiner would like to discuss the matter further, the undersigned may be contacted at (858) 350-8998.

Attached is a marked-up version of the changes being made by the current amendment.

Respectfully submitted,

Date: July 7, 2003

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 1, 3, 11-13, 15, 20, 22, 24, and 28 have been amended.

1. (Twice Amended) An integrated chip package, comprising:

at least one semiconductor chip having a first surface and a second surface;

an intermediate substrate electrically coupled via conductive bumps to the first surface of the at least one semiconductor chip;

a planar package substrate having a first surface electrically coupled to the intermediate substrate via a plurality of bonding wires, the intermediate substrate arranged above the planar package substrate; and

a heat sink having side portions extending towards the planar package surface, the heat sink thermally coupled to the second surface of the semiconductor chip so that heat generated from the at least one semiconductor chip flows towards the heat sink.

3. (Amended) The integrated chip package of Claim 1 wherein the heat sink is substantially thermally isolated from the planar package substrate.

11. (Amended) The integrated chip package of Claim 1 wherein the planar package substrate includes conductive pads on a second surface to electrically connect the integrated chip package to a circuit board via conductive bumps.

12. (Amended) The integrated chip package of Claim 1 further comprising a support material arranged between the planar package substrate and the intermediate substrate.

13. (Twice Amended) A method of forming an integrated chip package, comprising:

providing a semiconductor chip having a conductor pattern on a first surface;

electrically coupling the conductor pattern on the semiconductor chip to an intermediate substrate via a first set of conductive bumps;

providing a heat sink having side portions;

thermally coupling a second side of the semiconductor chip to [a] the heat sink so that heat generated from the semiconductor chip flows towards the heat sink;

arranging a planar package substrate below the intermediate substrate; and

electrically coupling the intermediate substrate to a first surface of [a] the planar package substrate via a plurality of bond wires.

15. (Amended) The method of Claim 13 further including thermally isolating the heat sink from the planar package substrate.

20. (Amended) The method of Claim 13 further including forming conductive pads on a second surface of the planar package substrate operable to electrically couple the integrated chip package to a circuit board via a second set of conductive bumps.

22. (Twice Amended) An integrated chip package, comprising:

at least one semiconductor chip configured for flip chip mounting, having a first surface and a second surface;

a planar package substrate having a first surface and a second surface, the planar package substrate second surface to electrically couple the integrated chip package to a circuit board via conductive bumps;

a flip chip conversion means arranged above the planar package substrate first surface and electrically coupled between the at least one semiconductor chip first surface and the planar package substrate first surface; and

a means for sinking heat from the second surface of the semiconductor chip so that heat generated from the semiconductor chip flows towards the means for sinking heat, the means for sinking heat having side portions extending towards the planar package substrate.

24. (Amended) The integrated chip package of Claim 22 further including means for thermally isolating the heat sinking means from the planar package substrate.

28. (Amended) The integrated chip package of Claim 22 wherein the second surface of the planar package substrate includes conductive pads for electrically interfacing to the conductive bumps.